HEWLETT hp PACKARD

OPERATING AND SERVICE MANUAL

13196A

PHASE-ENCODED TEST ACCESSORY

(FOR THE 7970E DIGITAL MAGNETIC TAPE UNIT)

Printed-Circuit Assemblies:

~~13196-60000, Series 1202~~
13196-60001, Series 1202

Options Covered

This manual covers option 001 as well as the standard HP 13196A Phase-Encoded Test Accessory.

13196-90000

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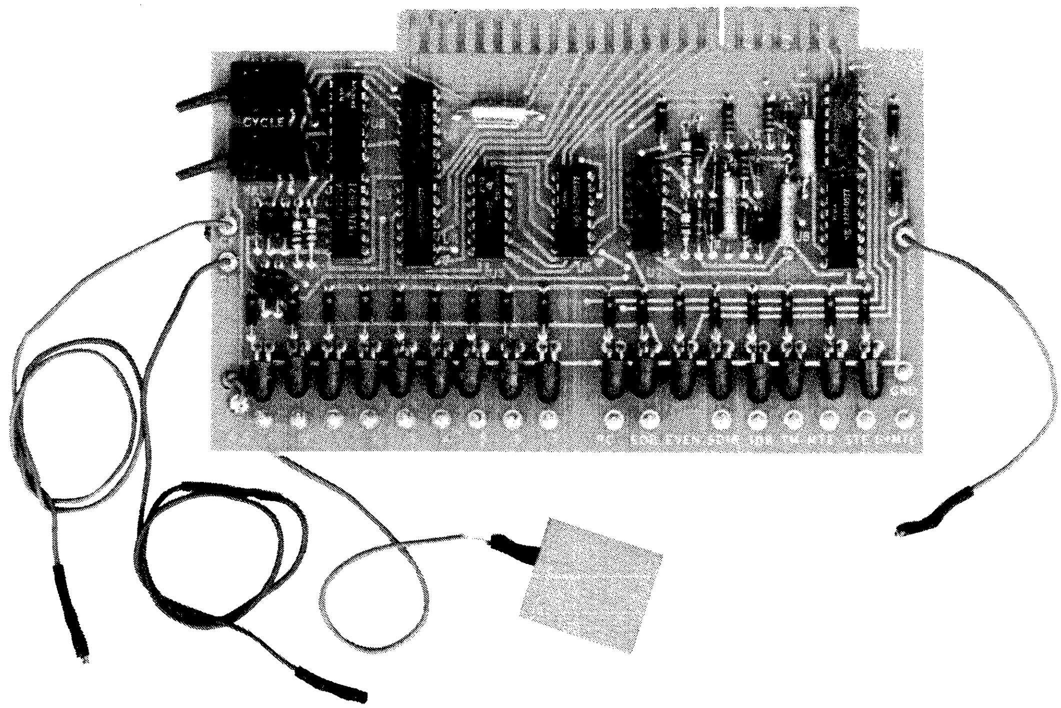
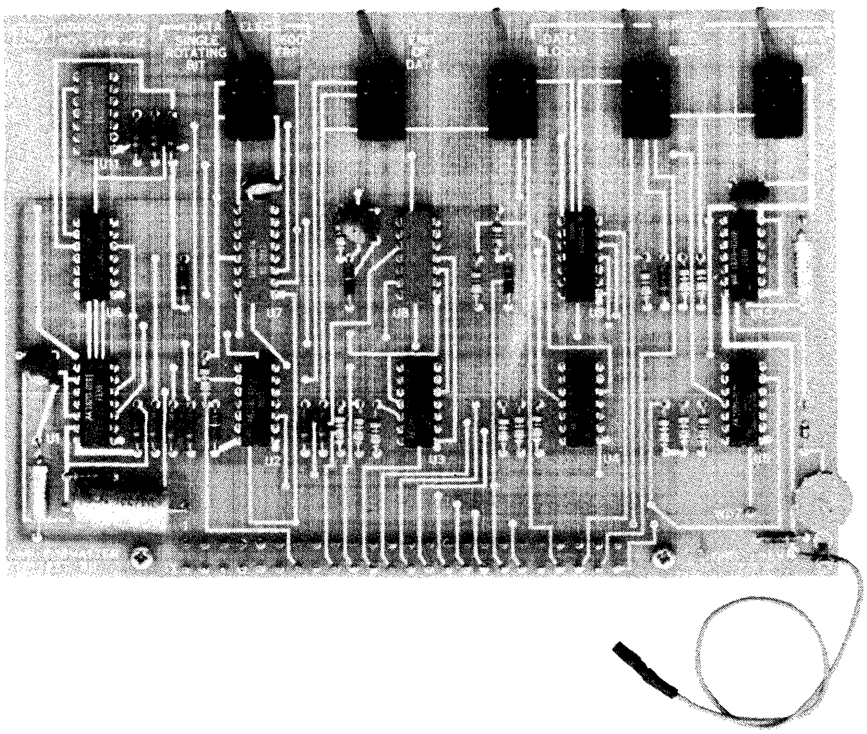


READ DATA TEST PCA



WRITE FORMATTER TEST PCA
(PART OF OPTION 001 ONLY)

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Figure 1-1. HP 13196A Phase-Encoded Test Accessory

GENERAL INFORMATION

SECTION I

1-1. INTRODUCTION.

1-2. This operating and service manual provides general information, installation, operation, theory of operation, and maintenance information for the HP 13196A and the HP 13196A Option 001 Phase-Encoded Test Accessories.

1-3. DESCRIPTION.

1-4. STANDARD TEST ACCESSORY.

1-5. The standard HP 13196A Phase-Encoded Test Accessory consists of a read data test printed-circuit assembly (PCA), part no. 13196-60000 (figure 1-1). It is used with the HP 13191A Control and Status Test Accessory to provide on-site, off-line maintenance capability for HP 7970E Digital Magnetic Tape Units (which uses phase-encoded electronics) operating in the read-only mode. The test accessory can be used with both master-only and master-slave configurations. The read data test PCA displays all signals present on the tape unit read connector and provides for operator selection of type and timing of tape-motion commands.

1-6. OPTION 001 TEST ACCESSORY.

1-7. The HP 13196A-001 Phase-Encoded Test Accessory consists of the read data test PCA previously mentioned and a write formatter test PCA, part no. 13196-60001 (figure 1-1). These two PCA's are used with the HP 13195A Write Formatter Accessory Kit as well as the HP 13191A Control and Status Test Accessory to extend the maintenance capability to HP 7970E tape units that include phase-encoded write circuits. The write formatter test PCA provides operator-selected writing of identification bursts (IDB's), tape marks (TM's), and a variety of test pattern data blocks.

1-8. IDENTIFICATION.

1-9. Hewlett-Packard uses five digits and a letter (00000A) for standard kit designations. If the designation of your kit does not agree with that on the title page of this manual, there are differences between your kit and the kit described in this manual. These differences are described in change sheets and manual supplements available at the nearest HP Sales and Service Office. These offices are listed at tne back of this manual.

1-10. Printed-circuit assembly (PCA) revisions are identified by a letter, a series code, and a division code stamped on the board (e.g., A-1152-22). The letter code identifies the version of the etched trace pattern on the unloaded board. The series code (four middle digits) refers to the electrical characteristics of the loaded assembly and the positions of the components. The division code (last two digits) identifies the Hewlett-Packard division which manufactured the PCA. If the series code stamped on the PCA does not agree with the series code shown on the schematic diagram in this manual, there are differences between the PCA and the PCA described in this manual. These differences are described in change sheets and manual supplements available at the nearest HP Sales and Service Office.

1-11. RELATED ACCESSORIES.

1-12. There are three test accessories used in conjunction with the phase-encoded (PE) test accessory. They are:

a. HP 13191A Control and Status Test Accessory.

b. HP 13195A Write Formatter Accessory Kit

c. Pre-written PE, ANSI format B test tape, part no. 5080-4555, or equivalent.

1-13. The control and status test accessory must always be used with the PE test accessory for testing either read or write electronics. The write formatter PCA (not to be confused with the write formatter test PCA, which is one of the two PCA's in the PE test accessory) need only be used when testing write electronics. The pre-written test tape provides test data for complete off-line testing of PE tape unit read circuits. This tape, or its equivalent, is required when using the standard PE test accessory, but is unnecessary when using the option 001 PE test accessory. With the option 001 test accessory, the tape written upon while testing write circuits can then be used to test read circuits. For a description of the format and the use of the pre-written test tape, refer to *HP 7970E Digital Magnetic Tape Unit Operating and Service Manual.*

1-14. RELATED MANUALS.

1-15. The following manuals contain information pertinent to other products associated with the PE test accessory.

a. *HP 7970E Digital Magnetic Tape Unit Operating and Service Manual*, part no. 07970-90765.

b. *HP 13191A Control and Status Test Accessory Manual Supplement*, part no. 13191-90000 (supplement to item a, above).

c. *HP 13194A Multiunit Cable Accessory Installation Manual*, part no. 13194-90003.

d. *HP 13195A Write Formatter Accessory Kit Operating and Service Manual*, part no. 13195-90000.

1-16. SPECIFICATIONS.

1-17. Specifications for the test accessories are listed in table 1-1.

Table 1-1. Specifications

POWER REQUIREMENTS	
Read Data Test PCA:	+5 Vdc @ 0.6A
Write Formatter Test PCA:	+5 Vdc @ 0.3A
LOGIC LEVELS	
Line Receivers (TTL)	
Logic 1 (High):	E ⩾ +2.4V @ I -2.6 mA (E = +3.6V @ I = zero A)
Logic 0 (Low):	E ⩽ +0.8V I ⩾ -9.6 mA
Line Transmitters (DTL)	
Logic 1 (High):	E = +5V @ I = zero A E ⩾ +2.4V @ I = -1.5 mA
Logic 0 (Low):	E ⩽ +0.4V @ I = 45 mA

SECTION II INSTALLATION

2-1. INTRODUCTION.

2-2. The HP 13196A Phase-Encoded Test Accessory is factory-checked to assure performance to published specifications before being packed for shipment. This section provides information to determine that the accessory has been received intact. Installation instructions for the PE test accessory and other associated tape unit accessory connections are included.

2-3. UNPACKING AND INSPECTION.

2-4. Before unpacking, inspect the shipping carton for damage. If damage to the shipping carton is evident, request that the carrier's agent be present when the accessory is unpacked. After unpacking, inspect the accessory for mechanical damage (cracks, broken parts, etc).

2-5. CLAIM FOR DAMAGE.

2-6. If the test kit is damaged and fails to meet published specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. (HP Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for the repair or replacement of the damaged test kit without waiting for any claims against the carrier to be settled.

2-7. INSTALLATION PREPARATION.

2-8. Turn off power on the tape unit to be tested (the master tape unit in master-slave multiunit applications) and take the tape unit physically off-line by removing the computer interface connector cables.

2-9. For testing read-only tape units, install a prerecorded test tape (PE, ANSI format "B" test tape, part no. 5080-4555, or equivalent) and install the HP 13191A Control and Status Test Accessory as described in *HP 13191A Control and Status Test Accessory Manual Supplement*.

2-10. For testing read-after-write tape units, install a reel of "scratch" tape with a write-enable ring (inspect tape pack for damage; do not use tape that shows signs of abuse), and install the HP 13191A Control and Status Test Accessory and the HP 13195A Write Formatter Accessory Kit as described in *HP 13191A Control and Status Test Accessory Manual Supplement*, and *HP 13195A Write Formatter Accessory Kit Operating and Service Manual*, respectively.

2-11. INSTALLATION.

2-12. Installing the HP 13196A and HP 13196A-001 test accessories involves plugging the read data test PCA into, and the write formatter test PCA onto the appropriate tape unit connectors.

2-13. READ DATA TEST PCA.

2-14. Insert the read data test PCA connector tongue into J14 of the master PE read motherboard assembly A22, part no. 07970-62040 (figures 2-1 and 2-2). (The connectors are keyed to prevent improper insertion.) Connect plug P1 of the +5 jumper J18 of motherboard A22 in the tape unit. Connect the CF and the CR jumpers to the HP 13191A Control and Status Test Accessory CF and CR test points, respectively. Set both read data test PCA switches away from the PCA's tongue connector, and connect the COND jumper to the PCA's GND test point.

2-15. WRITE FORMATTER TEST PCA.

2-16. Fit the write formatter test PCA onto the exposed tongue connector of the HP 13195A Write Formatter Accessory and connect the +5V power jumper onto WJ12 of the write motherboard assembly A17, part no. 07970-60230 (figures 2-1 and 2-2). Set all PCA switches to the left, and adjust the potentiometer to center range (approximately).

2-17. INSTALLATION CHECKOUT.

2-18. After installing the test PCA's, restore power to the tape unit, press the tape unit LOAD pushbutton, wait for LOAD indicator to light, and press the tape unit ON-LINE pushbutton. The SD16 indicator on the read data test PCA should be on, indicating PE mode selected and ready. The test accessory is now fully installed and ready for operation.

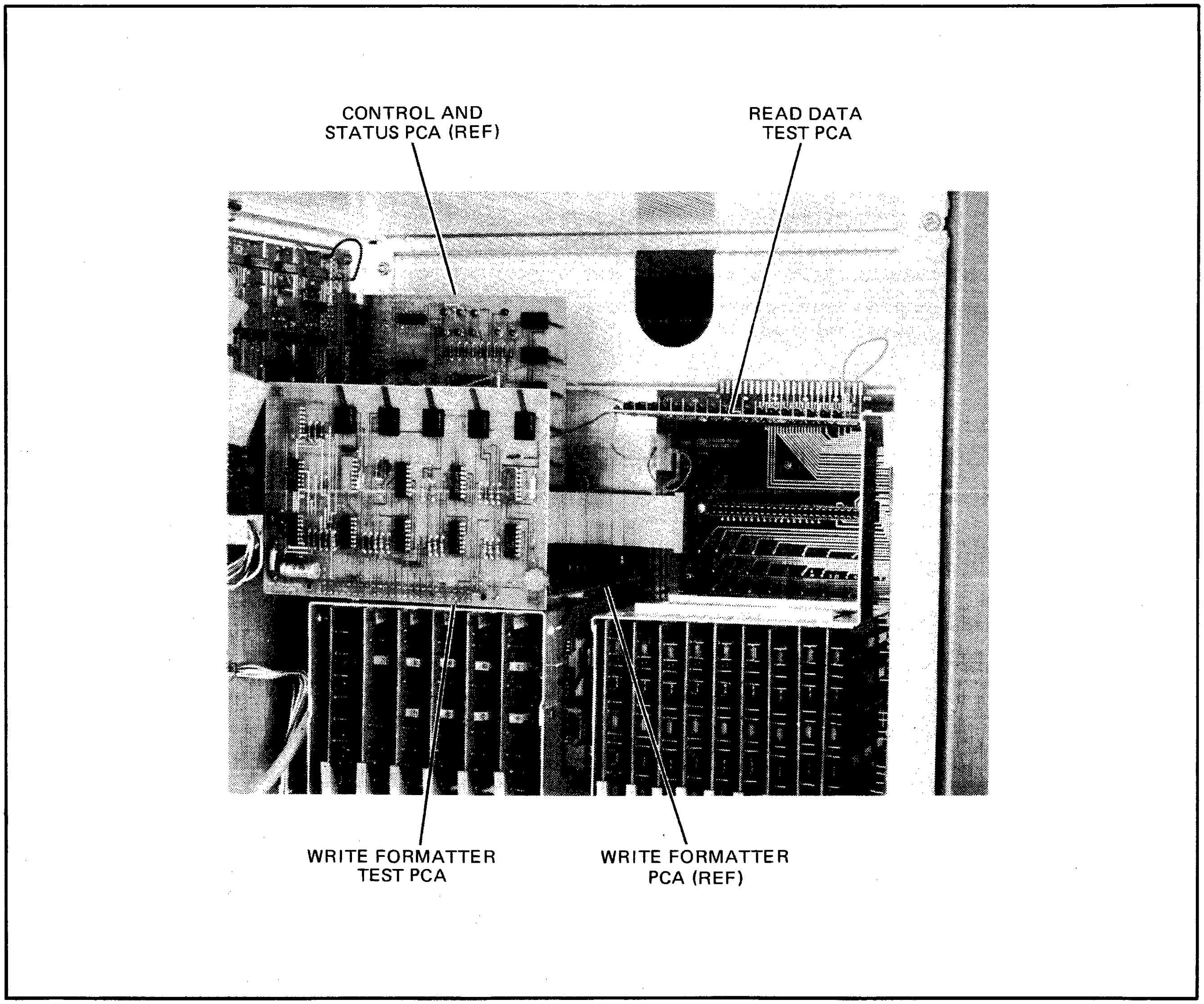

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Figure 2-1. Test Accessory Installation

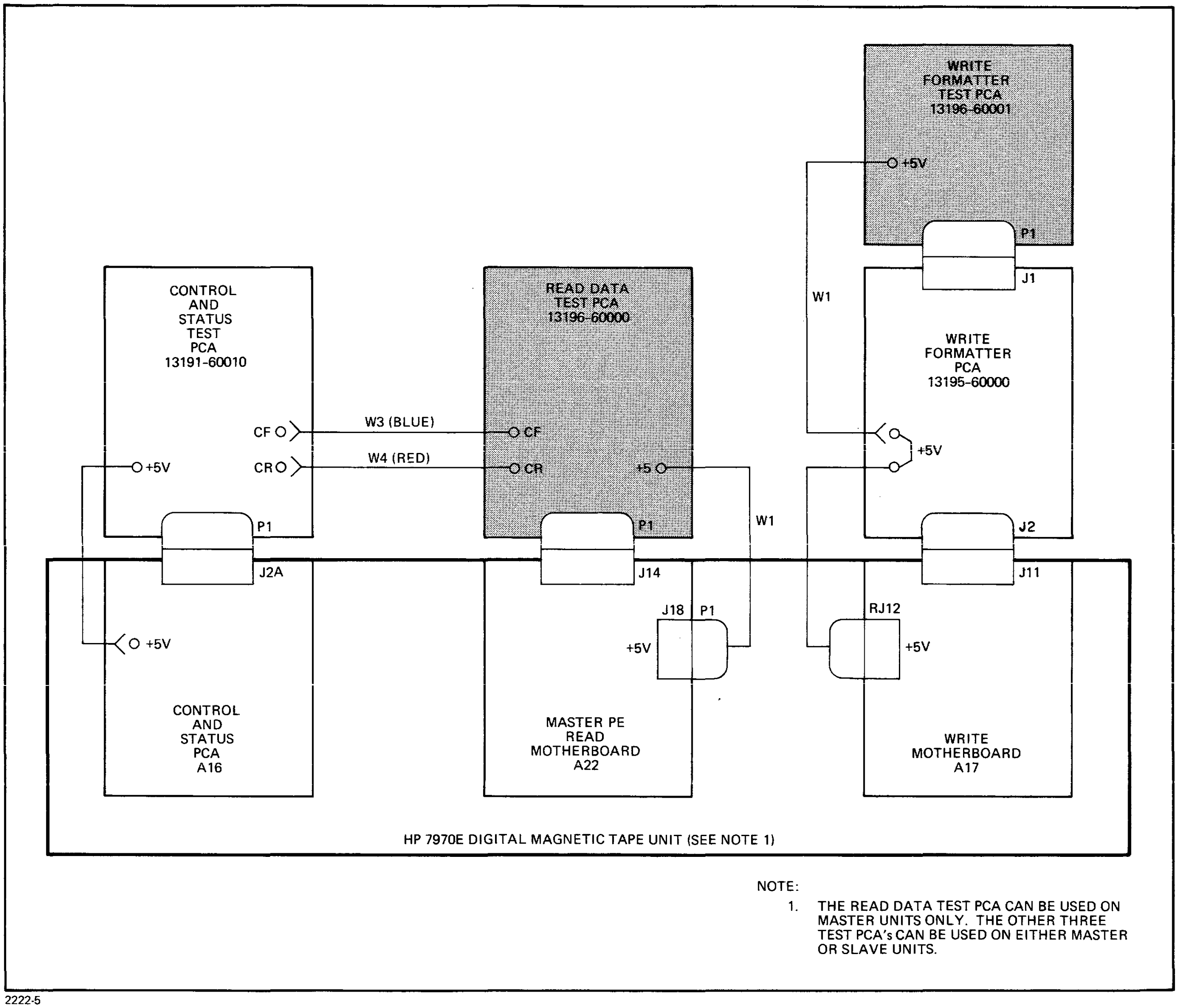

Figure 2-2. Test Accessory Interconnection Diagram

SECTION III OPERATION

3-1. INTRODUCTION.

3-2. This section contains information required to operate the HP 13196A and the HP 13196A Option 001 Phase-Encoded Test Accessories. All controls and indicators are identified, and the function of each is briefly described. The operation of each test PCA is covered separately. The descriptions of PCA operation are based on the assumption that the tape unit has been properly set up for testing in accordance with the *HP 7970E Digital Magnetic Tape Unit Operating and Service Manual*. No specific tests of the tape unit are included; these are contained within the above referenced manual.

3-3. CONTROLS AND INDICATORS.

3-4. Figure 3-1 points out the controls and indicators of the two test PCA's. Table 3-1 identifies the items called out in figure 3-1 and briefly describes the function of each.

3-5. READ DATA TEST PCA OPERATION.

3-6. The read data test PCA has 17 light-emitting diodes (LED's) that display the conditions (or, status of the signals) present on the tape unit read connector. The read data test PCA also supplies tape-motion commands to the tape drive control circuits. The PCA has controls that permit the operator to start and stop the tape manually, and to select a condition to automatically stop the tape after, or recycle the tape over, the detected condition.

Note: The controls on the read data PCA are used during read mode only.

3-7. Setting the ENABLE switch initiates forward tape motion. At the end of each data block read, the tape stops for approximately 150 milliseconds (end-of-block, or EOB, pause) and then resumes forward motion. If the COND jumper is not connected to a test point, the above described tape motion would continue until the ENABLE switch were reset, until the CF jumper were disconnected, or until the tape were to run off the supply reel, whichever came first. In the last case, the tape would automatically begin to rewind upon detection of the EOT marker if the control and status PCA had been previously set up to provide that function.

3-8. Connecting the COND jumper to one of the 17 test points along the near edge of the PCA, selects the condition that is to terminate the previously described tape motion. When the condition is detected, the test point goes to a "0". At the end of the data block in which the condition is detected, the tape motion is terminated in one of two ways, depending upon the position of the HALT/CYCLE switch.

3-9. Setting the HALT/CYCLE switch to HALT would cause the tape to remain stopped after the EOB pause. Setting the switch to CYCLE would cause the tape to continue to return to the start of the block and re-read it after each EOB pause.

Note: The HP 7970E can be made to read tape in the reverse direction during testing, by reversing the CF and the CR jumpers.

3-10. Assuming the ENABLE switch is set to the clear (near) position, there are only three steps to take to start a test:

a. Select the halt or the cycle mode (HALT/CYCLE switch).

b. Select the condition that is to trigger the selected mode (COND jumper to appropriate test point).

c. Set the ENABLE switch.

3-11. WRITE FORMATTER TEST PCA OPERATION.

3-12. The write formatter test PCA permits operator-controlled writing of identification bursts (IDB's), tape marks (TM's), or test pattern data blocks and insertion of operator-set, variable-length interrecord gaps between each block written. Setting the WSW and DRIVE switches on the control and status test PCA is required before operating the write formatter test PCA.

3-13. Setting the WRITE ID BURST switch initiates the writing of an identification burst (IDB) 3.5 inches long. It contains a total of 5,600 flux reversals, at 1,600 frpi (alternate "1's" and "0's"), in channel P, with reset flux state in channels 0 through 7. This IDB is followed alternately by gaps and new IDB's until the switch is reset.

3-14. Setting the WRITE TAPE MARK switch initiates the writing of a tape mark (TM). A tape mark consists of 80 flux reversals at 3,200 frpi (an "all 1's" pattern) in channels 0, 2, 5, 6, 7, and P, and dc erasure in channels 1, 3, and 4. This TM is followed alternately by gaps and new TM's until the switch is reset.

3-15. Setting the WRITE DATA BLOCKS switch initiates the writing of a preamble and a data test pattern. A preamble consists of 40 logic 0's followed by a logic 1 in all channels. The operator must select either a continuous

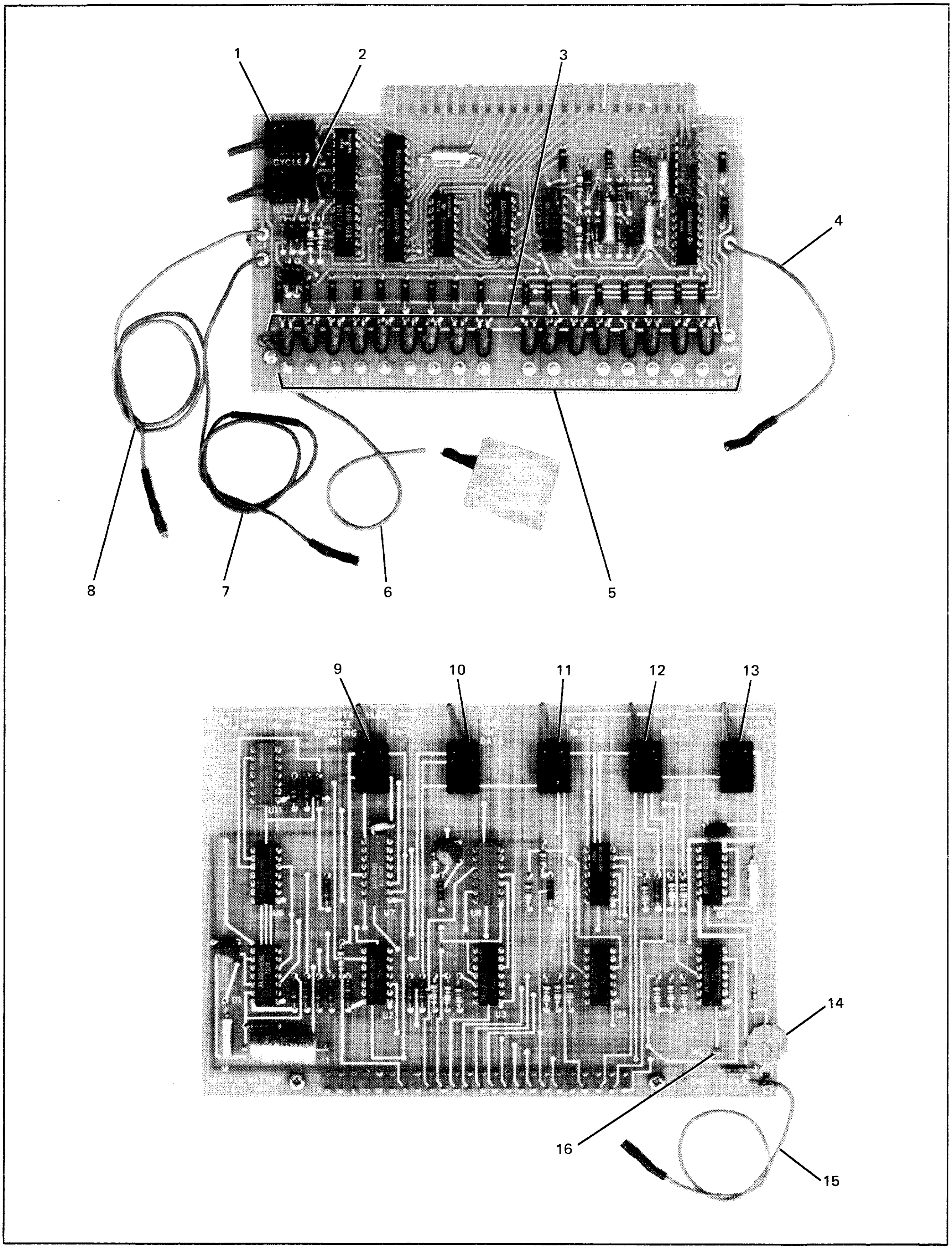

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Figure 3-1. Controls and Indicators

Table 3-1. Controls and Indicators

FIG. & INDEX NO.	NAME	REF DES	FUNCTION
READ DATA TEST PCA			
3-1, -1	ENABLE switch	S1	Controls (enables) tape motion.
-2	HALT/CYCLE switch	S2	Selects mode of terminating condition search.
-3	Left to right:		
	P indicator	CR7	Indicates detection of a "1" bit in track P.
	0 indicator	CR8	Indicates detection of a "1" bit in track 0.
	1 indicator	CR9	Indicates detection of a "1" bit in track 1.
	2 indicator	CR10	Indicates detection of a "1" bit in track 2.
	3 indicator	CR11	Indicates detection of a "1" bit in track 3.
	4 indicator	CR12	Indicates detection of a "1" bit in track 4.
	5 indicator	CR13	Indicates detection of a "1" bit in track 5.
	6 indicator	CR14	Indicates detection of a "1" bit in track 6.
	7 indicator	CR15	Indicates detection of a "1" bit in track 7.
	RC indicator	CR16	Indicates presence of read clock pulses.
	EOB indicator	CR17	Indicates detection of end of block.
	EVEN indicator	CR18	Indicates even vertical parity (error).
	SD16 indicator	CR19	Indicates selected tape unit is 1600-frpi density ready.
	IDB indicator	CR20	Indicates detection of identification burst block.
	TM indicator	CR21	Indicates detection of tape mark block.
	MTE indicator	CR22	Indicates detection of multiple-track error.
	STE indicator	CR23	Indicates detection of single-track error.
-4	COND jumper	W2	Provides means of inputting signal to initiate selected condition-search termination mode (halt or cycle mode). May be connected to any one of the following test points.
-5	Left to right:		
	P test point	TP1	Goes low when a "1" bit is detected in corresponding track. Stays low until a "0" bit is detected.
	0 test point	TP2	
	1 test point	TP3	
	2 test point	TP4	
	3 test point	TP5	
	4 test point	TP6	
	5 test point	TP7	
	6 test point	TP8	
	7 test point	TP9	
	RC test point	TP10	Alternates low and high in response to read clock.
	EOB test point	TP11	Goes low when end of block (postamble or preamble, depending on tape direction) is detected.
	SD16 test point	TP12	Goes low when selected tape unit is 1600-frpi density ready.
	IDB test point	TP13	Goes low when identification burst block is detected.
	TM test point	TP14	Goes low when tape mark block is detected.
	MTE test point	TP15	Goes low when multiple-track error is detected.
	STE test point	TP16	Goes low when single-track error is detected.
	S+MTE test point	TP17	Goes low when single-track or multiple-track error is detected.

Table 3-1. Controls and Indicators (Continued)

FIG. & INDEX NO.	NAME	REF DES	FUNCTION
READ DATA TEST PCA (Continued)			
-6	+5 jumper	W1	Provides means of inputting test PCA operating power (+5 Vdc).
-7	CR jumper	W4	Provides means of outputting reverse tape-motion command.
-8	CF jumper	W3	Provides means of outputting forward tape motion command.
WRITE FORMATTER TEST PCA			
-9	DATA SELECT switch	S5	Selects either single-rotating-bit or 1600-frpi data pattern.*
-10	END OF DATA switch	S4	Terminates the writing of a data block and initiates the writing of a postamble.
-11	WRITE DATA BLOCKS switch	S3	Initiates the writing of a preamble followed by a data block of the selected pattern.
-12	WRITE ID BURST switch	S2	Initiates the writing of identification burst blocks (one after another).
-13	WRITE TAPE MARK switch	S1	Initiates the writing of tape mark blocks (one after another).
-14	gap potentiometer	R1	Adjusts length of interrecord gap.
-15	+5V jumper	W1	Provides means of inputting test PCA operating power (+5 Vdc).
-16	WD7 test point	TP1	Provides a means of intentionally writing bad parity on tape by connecting test point to common.

*The pattern written on tape may be neither of these two, depending on position of other switches. For details, see paragraphs in this section dealing jointly with switches S3, S4, and S5.

single rotating bit (SRB) data block, a continuous data block of alternate "1's" and "0's" in all channels, a continuous data pattern of alternate "1's" and "0's" in channels 0 through 7 with all "1's" in channel P, a nine-character SRB data block, or a zero-length data block. The continuous data test patterns are terminated by resetting the WRITE DATA BLOCKS switch at which time the writing of a postamble is initiated to complete the data block. A postamble is a logic 1 followed by 40 logic 0's in all channels. The individual SRB and zero-length data patterns are automatically followed by a postamble, and then alternately by gaps and new patterns until the WRITE DATA BLOCKS switch is reset.

3-16. Setting the DATA SELECT SINGLE ROTATING BIT and WRITE DATA BLOCKS switches initiates the writing of a preamble, followed by continuous SRB data blocks, as shown in figure 4-2.

3-17. Setting the DATA SELECT 1600 FRPI and WRITE DATA BLOCKS switches initiates the writing of a preamble, followed by a continuous data block of alternate "1's" and "0's" (1,600 frpi) in all channels, as shown in figure 4-2.

3-18. The continuous data block of alternate "1's" and "0's" in all channels can be written only if the jumper on the HP 13195A Write Formatter Accessory is in position 3. This pattern is useful for adjusting the tape unit read-after-write preamp gain and write-skew delay. However, since this pattern generates even parity in every other nine-bit byte, detected error conditions displayed on the read data test PCA must be ignored.

Note: A continuous data pattern of alternate "1's" and "0's" in channels 0 through 7 with all "1's" (3,200 frpi) in channel P can be selected by changing the jumper on the HP 13195A Write Formatter Accessory to position 4. Because this pattern generates odd parity (an odd number of bits written) in each nine-bit byte, error conditions displayed on the read data test PCA are valid.

3-19. Setting the DATA SELECT SINGLE ROTATING BIT, END OF DATA, and WRITE DATA BLOCKS switches initiates the writing of one complete data block with a preamble, an SRB data pattern, and a postamble, followed alternately by gaps and new data blocks. (Resetting the END OF DATA switch results in the subsequent writing of continuous SRB data blocks.)

3-20. Setting the DATA SELECT 1600 FRPI, END OF DATA, and WRITE DATA BLOCKS switches initiates the writing of one complete data block with a preamble, a zero-length data pattern, and a postamble, followed alternately by gaps and new data blocks. (Resetting the END OF DATA switch results in the subsequent writing of a continuous 1600-frpi data block.)

3-21. Connecting a jumper between common (GND test point TP2) and WD7 test point TP1 and setting the DATA SELECT SINGLE ROTATING BIT and WRITE DATA BLOCKS switches, initiates the writing of bad parity on the tape. This is intentional, in order to be able to later read this tape to check the parity error detection circuits of the tape unit under test.

THEORY OF OPERATION — SECTION IV

4-1. INTRODUCTION.

4-2. This section describes the theory of operation of the read data test PCA and the write formatter test PCA. See the foldout schematic diagrams in the maintenance section for illustration of the circuits described in this section. The signal names for the mnemonics used in this section are located on the apron of the respective schematic diagram.

4-3. READ DATA TEST PCA.

4-4. The read data test PCA is a piggyback PCA that displays the status of signals on the tape unit read connector and controls tape motion during read mode. The operator can control tape-motion manually, or select automatic control in response to selected read signals. To provide the display of, and tape-motion control in response to, the various read signals, the read data test PCA has 17 indicators and a search-and-cycling circuit. (Display of an even-parity condition of the nine read data lines is also provided.)

4-5. READ SIGNAL INDICATORS.

4-6. All read signal indicators, except the EVEN, the RC, and the EOB indicators, are illuminated when the corresponding signals are asserted, and stay illuminated for the duration of signal assertion. The EVEN, RC, and EOB indicators are illuminated when their corresponding signals are asserted and stay illuminated for about 150 milliseconds; the three signals are so short in duration that "pulse-stretcher" circuits (timed one-shot multivibrators) are used to allow observation of the assertions.

4-7. SEARCH-AND-CYCLING CIRCUIT.

4-8. With ENABLE switch S1 off, a logic 0 is applied to the clear input of flip-flop U2B; the set-side output of U2B in turn clears flip-flop U2A. The logic 0 is also applied through diode CR7 to clear flip-flop U1; the clear-side output of U1 satisfies the input of "nand" gate U3D and the output of U3D is inverted through U6C to enable the inputs of "nand" gates U3A and U3C. The clear-side output of U2A satisfies the input of U3C, and the set-side output of U2A satisfies the input of U3A.

4-9. ASSERTED-SIGNAL CONDITION SEARCH. Setting ENABLE switch S1 to the ENABLE position allows the low output of U3C to be applied to the tape unit as the $\overline{\text{CF}}$ signal. Tape motion then proceeds forward, halting for about 150 milliseconds (due to one-shot multivibrator U7A) each time an end-of-block signal is detected. (A low $\overline{\text{EOB(E)}}$ signal from the clear-side of U7A is doubly inverted by U3D and U6C and disables both command output gates, U3A and U3C.)

4-10. ASSERTED-SIGNAL CONDITION DETECTION. Receiving a low, asserted-signal condition through COND jumper W2 clocks and sets flip-flop U2B. The set-side output of U2B and the clear-side output of flip-flop U2A enable the set-side input of flip-flop U1. At the end of the next block, the $\overline{\text{EOB}}$ signal goes low, clocking flip-flop U1. The flip-flop will either be set or stay cleared depending on the position of the HALT/CYCLE switch.

4-11. ASSERTED-SIGNAL CONDITION HALT. Setting CYCLE/HALT switch S2 to the HALT position allows flip-flop U1 to be set when the low $\overline{\text{EOB}}$ clock input is received. The set-side output of U1 disables "nand" gate U3D and the high output of U3D is inverted through U6C to disable "nand" gates U3A and U3C to inhibit any motion command to the tape unit.

4-12. ASSERTED-SIGNAL CONDITION CYCLING. Setting CYCLE/HALT switch S2 to the CYCLE position clears flip-flop U1 regardless of its clock input. The clear-side output of U1 keeps the inputs of "nand" gates U3A and U3C enabled through "nand" gate U3D and inverter U6C. The high-to-low transition of the $\overline{\text{EOB}}$ signal clocks and sets flip-flop U2A through inverter U4D. The set-side output of U2A satisfies the input of U3A and the low output of U3A is applied to the tape unit as the $\overline{\text{CR}}$ signal. After the tape reverses motion and the beginning of the block is detected, the $\overline{\text{EOB}}$ signal again goes low (since the reverse reading of a phase-encoded preamble is interpreted as a postamble). The high-to-low transition of the $\overline{\text{EOB}}$ signal clocks and clears U2A to re-initiate the $\overline{\text{CF}}$ signal to the tape unit. Tape motion cycles back and forth over the block in which the asserted-signal condition until S2 is set to HALT, or S1 is reset.

Note: While cycling over an asserted-signal condition, resetting ENABLE switch S2 will stop the tape, but there is little control over the place it stops and direction of travel prior to stopping. To stop the tape and leave it ready to go on to further data blocks, first set the HALT/CYCLE switch to HALT and wait for the tape to stop. When it does, it will be at the end of the block in which the asserted-signal condition was detected. If the ENABLE switch is now reset, then set again, the tape will move forward, leaving the old data block and proceeding to those further on. Between resetting it again, the operator has option of selecting a new test point for the COND jumper and of selecting the cycle function again.

4-13. WRITE FORMATTER TEST PCA.

4-14. The write formatter test PCA is a piggyback PCA that plugs onto the HP 13195A Write Formatter Accessory to provide operator-controlled writing of tape mark (TM) blocks, identification burst (IDB) blocks, and a selection of five test pattern data blocks. The five available test patterns are a continuous, single rotating bit (SRB) data pattern, a continuous data pattern of alternate "1's" and "0's" (1,600 frpi) in all channels, a continuous data pattern of alternate "1's" and "0's" in channels 0 through 7 with all "1's" (3,200 frpi) in channel P, an individual SRB data pattern, and a zero-length data pattern. A preamble precedes each data pattern and a postamble follows each data pattern to make a complete data block. An interrecord gap separates each written block, and is of a variable, operator-controlled length. Tables 4-1 and 4-2 show an SRB pattern and a 1600-frpi pattern, respectively.

Note: The alternate "1's" and "0's" (1600-frpi pattern) in all channels is useful for adjusting the tape unit read-after-write preamp gain and write-skew delay; however, since even parity is generated in every other nine-bit byte, detected error conditions displayed on the read data test PCA should be ignored.

Table 4-1. Single Rotating Bit (SRB) Pattern

TRACK	TIME SEQUENCE								
	1	2	3	4	5	6	7	8	9
P	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0
2	0	0	0	1	0	0	0	0	0
3	0	0	0	0	1	0	0	0	0
4	0	0	0	0	0	1	0	0	0
5	0	0	0	0	0	0	1	0	0
6	0	0	0	0	0	0	0	1	0
7	0	0	0	0	0	0	0	0	1

Table 4-2. 1600 Flux Reversals Per Inch (FRPI) Pattern

TRACK	TIME SEQUENCE								
	1	2	3	4	5	6	7	8	9
P*	0	1	0	1	0	1	0	1	0
0	0	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	0	1	0
2	0	1	0	1	0	1	0	1	0
3	0	1	0	1	0	1	0	1	0
4	0	1	0	1	0	1	0	1	0
5	0	1	0	1	0	1	0	1	0
6	0	1	0	1	0	1	0	1	0
7	0	1	0	1	0	1	0	1	0

*Alternate ones and zeros (1,600 frpi) is shown in channel P; this is accomplished by having the jumper on the HP 13195A Write Formatter Accessory in position 3. All ones (3,200 frpi) in channel P can be generated by having the jumper in position 4.

4-15. To provide the various writing functions, the write formatter test PCA has five main circuits: the sequence control circuit, data pattern select circuit, SRB generate circuit, 1600-frpi generate circuit, and end-of-data circuit.

4-16. SEQUENCE CONTROL CIRCUIT.

4-17. The sequence control circuit controls the sequence of four operational states: the clear state, command-enable state, end-of-data state, and gap-generate state. The outputs of flip-flops U1A and U1B determine these four operational states (figures 4-1 and 4-2). (Since the operation of all other test PCA circuits occurs during the operation of the sequence control circuit, the sequence control circuit theory of operation will be discussed according to its four operational states.)

4-18. SEQUENCE CONTROL CIRCUIT (CLEAR STATE).

4-19. The clear state (U1A clear, U1B clear) is the initial state for all test PCA operations. When power is first applied, capacitor C3 applies a logic 0 ($\overline{\text{POP}}$ signal) to the clear-side inputs of U1A and U1B to initialize the sequence control circuit. The clear-side outputs of U1A and U1B satisfy the inputs of "nand" gate U11C, which issues a low $\overline{\text{CLR}}$ signal to initialize the pattern select and the two pattern generate circuits.

4-20. SEQUENCE CONTROL CIRCUIT (COMMAND-ENABLE STATE)

4-21. Setting any of the three WRITE switches (TAPE MARK switch S1, ID BURST switch S2, or DATA BLOCKS switch S3) initiates the command-enable state (U1A set, U1B clear) by satisfying the input of "and" gate U6C which sets flip-flop U1A. The set-side output of U1A and the clear-side output of U1B satisfy the inputs of "nand" gate U9A, which generates a low $\overline{\text{CEN}}$ signal. This signal becomes the $\overline{\text{WTM}}$, the $\overline{\text{WID}}$, or the $\overline{\text{WPA}}$ signal, depending on which WRITE switch is set.

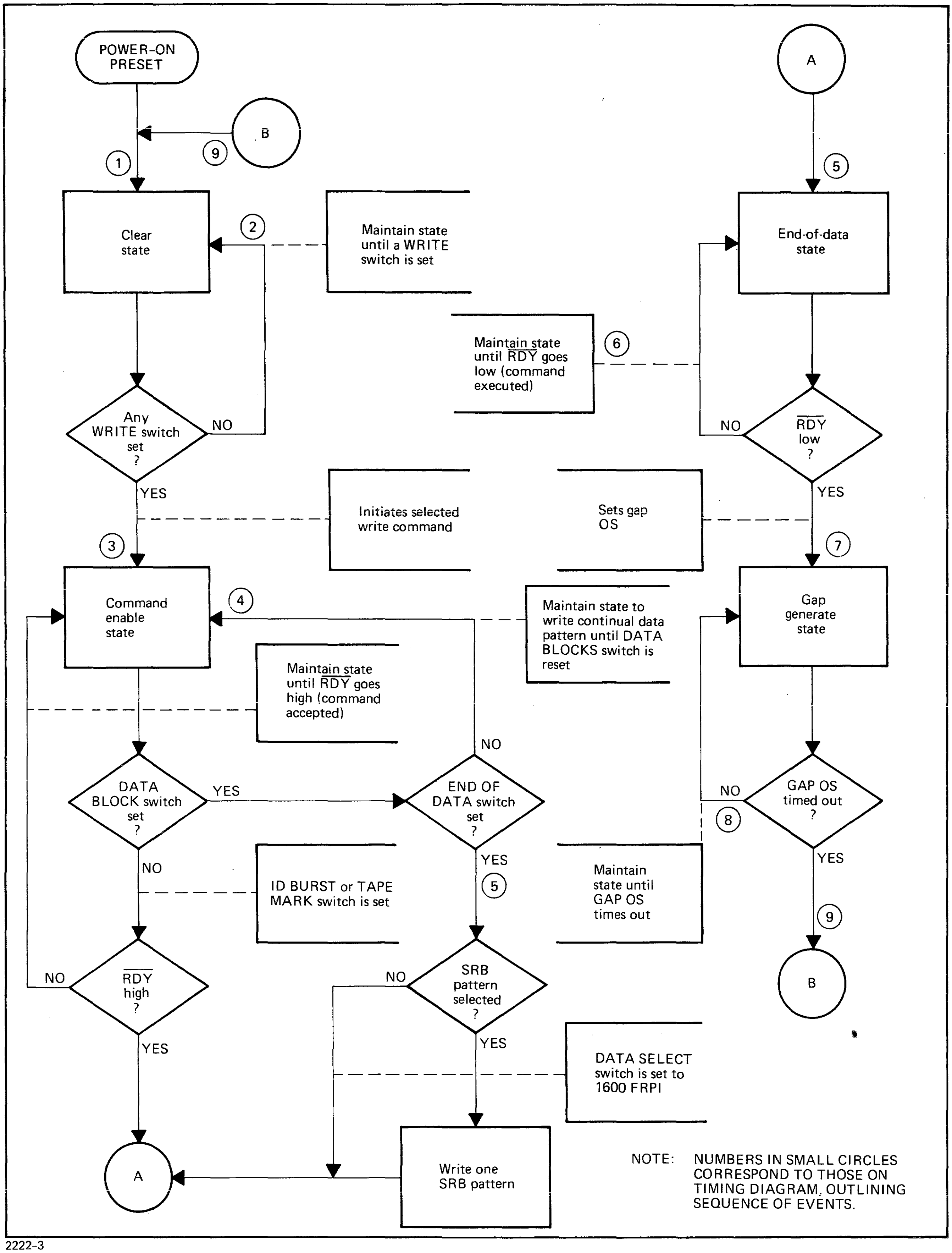


Figure 4-1. Write Formatter Test PCA Control Sequence Flow Diagram

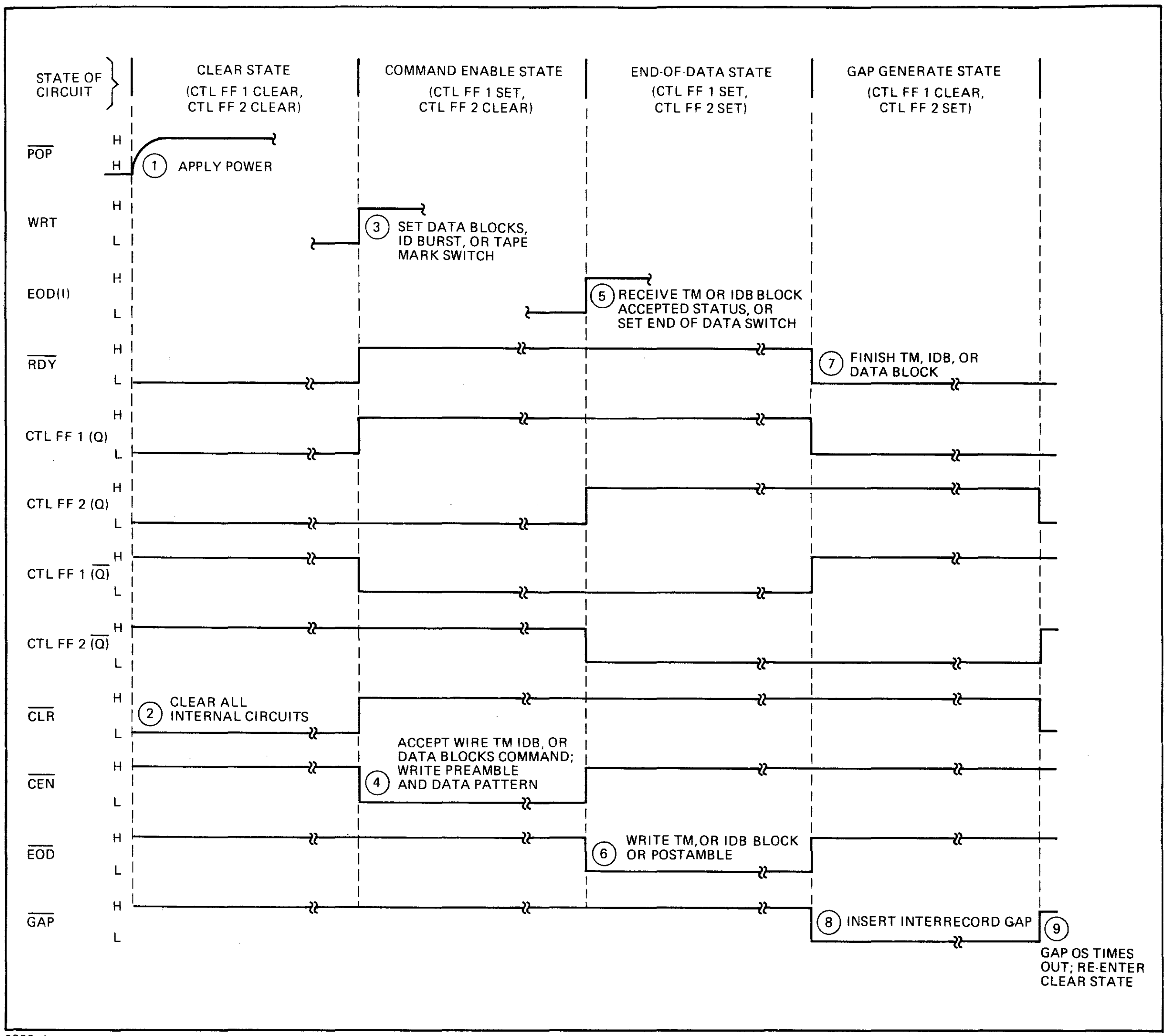


Figure 4-2. Write Formatter Test PCA Timing Diagram

4-22. If the $\overline{\text{WTM}}$ signal is given, the write formatter accessory writes a tape mark block on the tape. This block consists of 40 "0's" in channels P, 0, 2, 5, 6, and 7, with a reset flux state in channels 1, 3, and 4 (IBM format). If the $\overline{\text{WID}}$ signal is given, the write formatter assembly writes an identification burst block on the tape. This block consists of 5,600 characters (at 1,600 frpi) of alternate "1's" and "0's" in channel P, with a reset flux state in all other channels. If the $\overline{\text{WPA}}$ signal is given, the write formatter accessory writes a preamble followed by one of the five available data patterns. At the end of the data pattern, the write formatter accessory writes a postamble. (Refer to the discussion of the end-of-data circuit for details.) The preamble consists of 40 "0's" followed by a single "1" in all channels. The postamble consists of a single "1" followed by 40 "0's" in all channels. The write formatter accessory acknowledges receipt of one of these three command signals by making the $\overline{\text{RDY}}$ signal go high. It acknowledges that execution of the command is complete by making the $\overline{\text{RDY}}$ signal go low.

4-23. DATA PATTERN SELECT CIRCUIT.

4-24. The data pattern select circuit provides a logic 1 input either to the SRB generate circuit and end-of-data circuit, or to the 1600-frpi generate circuit. Setting DATA SELECT switch S5 to SINGLE ROTATING BIT initiates the SRB signal during the clear state of the sequence control circuit. The low $\overline{\text{CLR}}$ signal is connected through S5 to the input of "nand" gate U11A, and the output of U11A, the SRB signal, goes high. Setting S5 to 1600 FRPI unconditionally initiates the 1600 signal. A logic 0 is connected through S5 to the input of "nand" gate U11B, and the output of U11B, the 1600 signal, goes high.

Note: The latching of the SRB signal by cross-coupled "nand" gates U11A and U11B is retained regardless of the selected position of DATA SELECT switch S5, until the next clear state of the sequence control circuit occurs. (Toggling END OF DATA switch S4 causes the sequence control circuit to return to the clear state; refer to the discussion on the end-of-data circuit for details.)

4-25. SRB GENERATE CIRCUIT.

Note: In paragraphs 4-26 and 4-27 it should be noted that the data bits written on the tape are the same as the data bits out of the selected pattern generate circuit, prior to inversion by the DTL line transmitters (U3, U4, and U5). The data bits at the output pins of the test PCA are the complement of the bits written on the tape.

4-26. The SRB generate circuit uses SRB flip-flop U7A and parallel-out, eight-bit shift register U8 to generate a single rotating bit pattern. At the initialization of the clear state, U8 is cleared, and SRB flip-flop U7A is set to enable U8, and to make $\overline{\text{WDP}}$ go low at the data lines. With WRITE DATA BLOCKS switch S3 set, DATA SELECT switch S5 set to SINGLE ROTATING BIT, and the sequence control circuit in the command-enable state, the write formatter accessory generates a preamble. Upon completion of the preamble, the write formatter accessory writes the data available at the data lines (a "1" in channel P and "0's" in all other channels initially). The write formatter accessory acknowledges receipt of the data by making the $\overline{\text{DA}}$ signal go low, which in turn clocks U7A and U8 to shift the position of the "1" from channel P to channel 0. The data is received, $\overline{\text{DA}}$ goes high, and U8 is again clocked to shift the position of the "1" from channel 0 to channel 1. (Since the set- and clear-side inputs of U7A are now both low, succeeding low-going $\overline{\text{DA}}$ clocks will not change the state of U7A until the "1" in register U8 is rotated to channel 7.) After the "1" is rotated to channel 7, register U8 will not re-initiate the "1" in channel 0 until its input is re-enabled. When the "1" in channel 7 is applied to the set-side input of U7A, the next low-going $\overline{\text{DA}}$ clock sets U7A. Flip-flop U7A re-enables register U8 and re-initiates the "1" in channel P to begin another pattern. The SRB pattern is generated continuously until the end-of-data state is set.

4-27. 1600-FRPI GENERATE CIRCUIT.

4-28. The 1600-frpi generate circuit is a divide-by-two flip-flop that alternately applies "1's" and "0's" to all nine data lines by frequency-dividing the $\overline{\text{DA}}$ signal from the write formatter accessory. At the initialization of the clear state, 1600 flip-flop U7B is cleared and the low output from the set side makes all nine data lines go high. With WRITE DATA BLOCKS switch S3 set, DATA SELECT switch S5 set to 1600 FRPI, and the sequence control circuit in the command-enable state, the write formatter accessory generates a preamble. Upon completion of the preamble, the write formatter accessory writes the data available at the data lines ("0's" in all channels initially). The write formatter accessory acknowledges receipt of the data by making the $\overline{\text{DA}}$ signal go low. The $\overline{\text{DA}}$ signal sets U7B and the high output from the set side now makes all nine data lines go low. When the next low $\overline{\text{DA}}$ signal clears U7B, the clear-side output of U7B makes the data lines go high to repeat the pattern. The 1600-frpi pattern is generated continuously until the end-of-data state is set.

Note: With the jumper of the HP 13195A Write Formatter Accessory in position 3, the 1600-frpi (alternate "1's" and "0's") pattern is written in all channels as received from the test PCA. With the jumper in position 4, the write formatter accessory disregards the $\overline{\text{WDP}}$ signal from the test PCA and sums the number of "1's" received from all other channels in each byte. The write formatter accessory generates a "1" in channel P if the sum is even, and a "0" if the sum is odd; since alternate "1's" and "0's" in eight channels always yields an even number of "1's" (8 or 0), a "1" will always be generated in channel P unless a parity error occurs.

4-29. END-OF-DATA CIRCUIT.

4-30. The end-of-data circuit provides the EOD(I) signal to advance the sequence control circuit into its end-of-data state. The end-of-data circuit initiates the end-of-data state of the sequence control circuit whenever a $\overline{\text{WTM}}$ or a $\overline{\text{WID}}$ signal has been accepted, or a data pattern is terminated through the setting of END OF DATA switch S4.

4-31. The high $\overline{\text{RDY}}$ signal from the write formatter acknowledging receipt of the $\overline{\text{WTM}}$ or the $\overline{\text{WID}}$ signal satisfies the input of "nand" gate U9D. The low output of U9D is inverted through U2A to initiate the end-of-data state of the sequence control circuit.

4-32. Setting END OF DATA switch S4 terminates any of the five data patterns by accepting the low output of either "nand" gate U9C or inverter U2C. In terminating the continuous or the individual SRB pattern, the high $\overline{\text{DA}}$ signal (following the low $\overline{\text{DA}}$ signal that denotes acceptance of write data bit 6) and the high channel 7 output (Q_7) of register U8 satisfy the inputs of "nand" gate U9C, which provides a low output through S4. The low output through S4 is inverted through U2A to initiate the end-of-data state of the sequence control circuit. In terminating the continuous 1600-frpi patterns or the zero-length pattern, the low SRB command, resulting from having set DATA SELECT switch S5 to 1600 FRPI, is inverted through U2D and inverted again through U2C, which provides a low output through S4.

4-33. SEQUENCE CONTROL CIRCUIT (END-OF-DATA STATE).

4-34. The end-of-data state (U1A set, U1B set) makes the $\overline{\text{EOD}}$ signal to the write formatter accessory go low. (The high output of inverter U2A from the end-of-data circuit satisfies the input of "and" gate U6D and sets flip-flop U1B. The set-side outputs of flip-flops U1A and U1B satisfy the inputs of "nand" gate U9B, causing the $\overline{\text{EOD}}$ signal to the write formatter accessory to go low.)

Note: The $\overline{\text{EOD}}$ signal is used only to end the writing of data blocks and is disregarded by the write formatter accessory when writing the automatically ended tape mark or identification burst block. In either disregarded case, the set-side output of U1B serves only to prepare the sequence control circuit for the gap-generated state.

4-35. Receiving the low $\overline{\text{EOD}}$ signal causes the write formatter accessory to terminate acceptance of any more data and initiates the writing of a postamble. Completion of the postamble causes the sequence control circuit to advance to the gap-generate state.

4-36. SEQUENCE CONTROL CIRCUIT (GAP-GENERATE STATE).

4-37. The gap-generate state (U1A clear, U1B set) enables the generation of an interrecord gap that separates each written block for a duration of 10 to 160 milliseconds (±10 percent), depending on the position of potentiometer R1. The potentiometer can be adjusted by the operator. Upon completion of a tape mark block, an identification burst block, or the postamble of a data block, the $\overline{\text{RDY}}$ signal from the write formatter PCA goes low. The ready status is inverted through U2B to satisfy the input of "and" gate U6B and clear flip-flop U1A. The clear-side output of U1A and the set-side output of flip-flop U1B trigger one-shot multivibrator U10. The $\overline{\text{GAP}}$ signal out of the clear side of U10 goes low for a length of time determined by the position of potentiometer R1. When U10 times out, the $\overline{\text{GAP}}$ signal goes high, which satisfies the input of "and" gate U6A which, in turn, reinitiates the clear state by clearing flip-flop U1B.

MAINTENANCE

5-1. INTRODUCTION.

5-2. This section contains maintenance information for the HP 13196A and the HP 13196A-001 Phase-Encoded Test Accessories. Included are preventive maintenance and troubleshooting information. Parts lists and parts location and schematic diagrams are provided as an aid to troubleshooting.

5-3. PREVENTIVE MAINTENANCE.

5-4. Detailed preventive maintenance procedures and schedules are provided in the HP computer documentation for the computer and tape unit; there are no separate preventive maintenance procedures for the test accessory.

5-5. TROUBLESHOOTING.

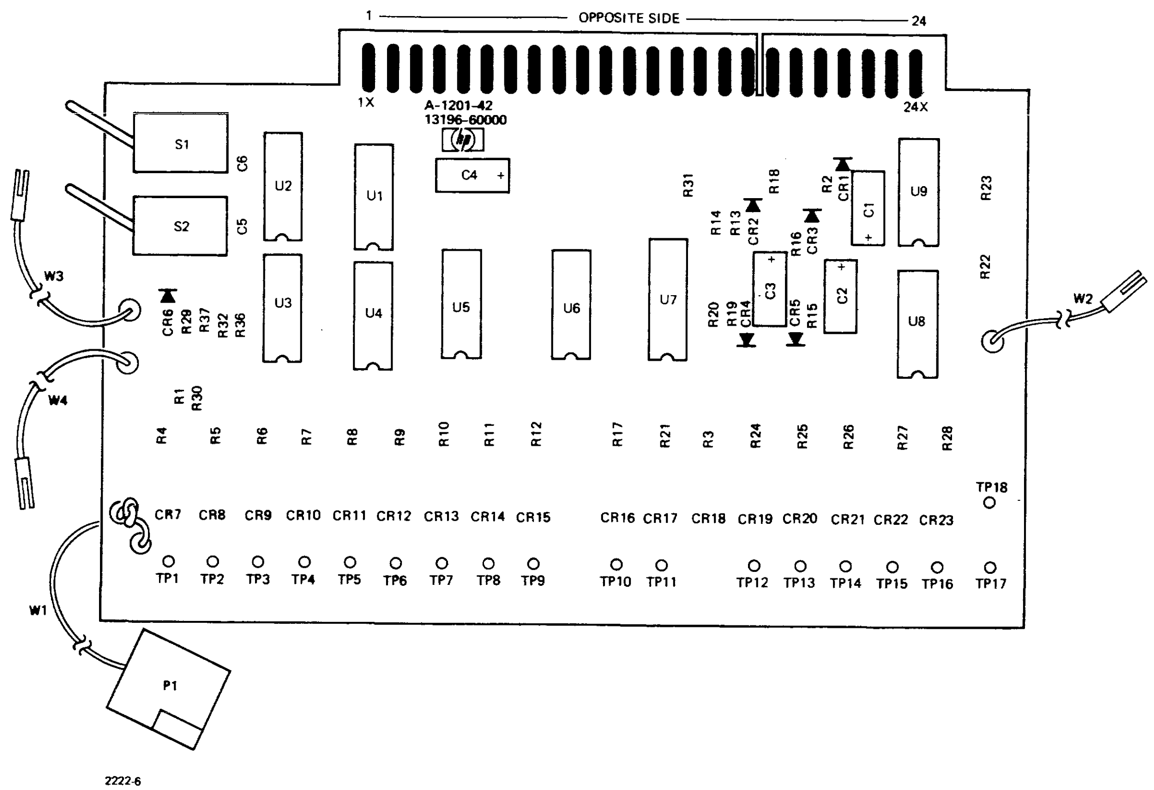
5-6. Troubleshooting for the test accessory is accomplished by analyzing improper operation determined according to the operation and the theory of operation sections. To further isolate the trouble, refer to the parts location and schematic diagrams in figures 5-1 and 5-2, and to the maintenance aids described below.

5-7. Tables 5-1 and 5-2 are parts lists for the read data test PCA and the write formatter test PCA, respectively. The parts are listed in alphanumeric order by reference designation.

5-8. Figure 5-3 contains logic diagrams and pin locations for the integrated circuits used on the test PCA's. Table 5-3 gives the integrated-circuit input levels, output levels, and delay times that correspond to the characteristic number shown below each diagram in figure 5-3.

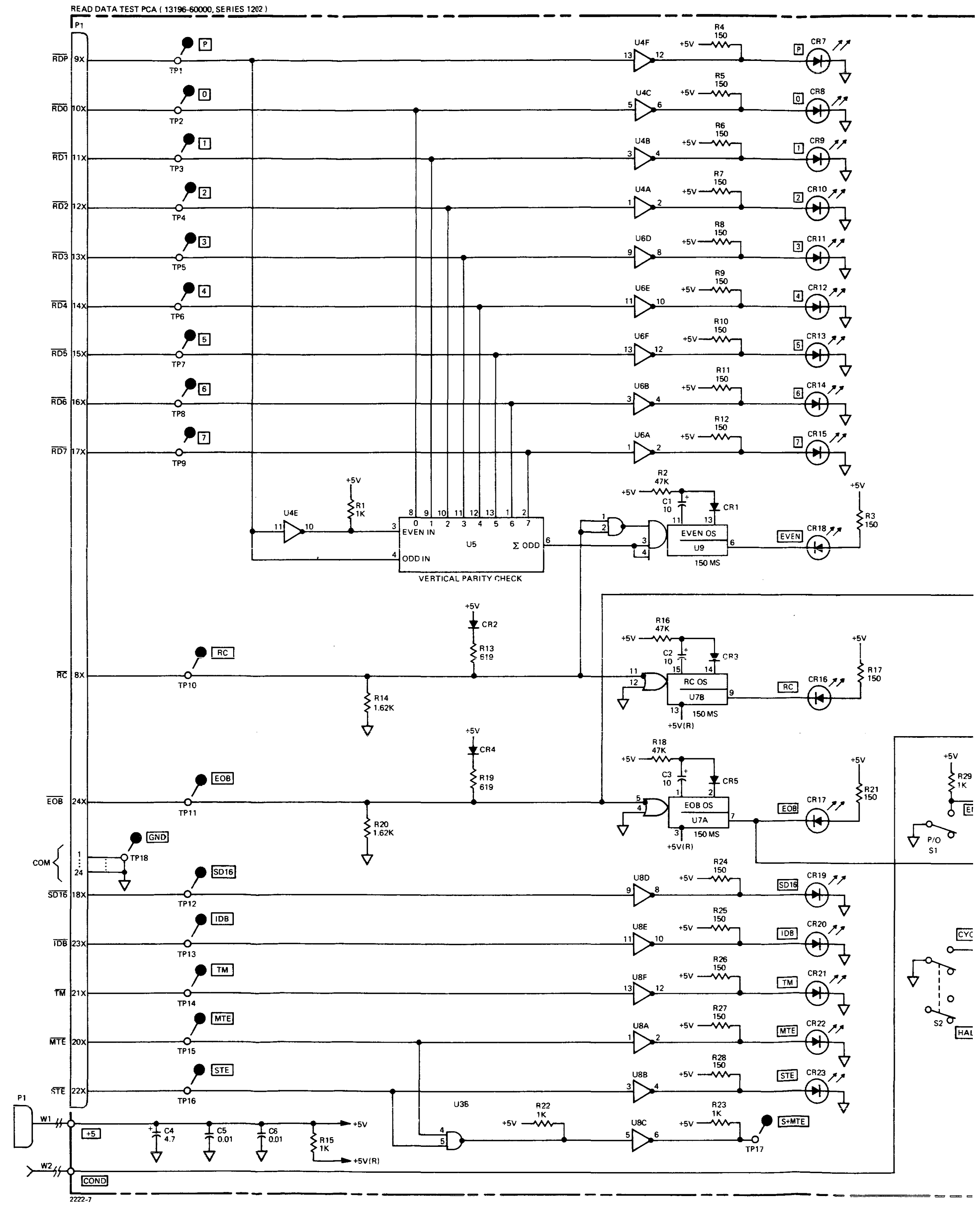
Table 5-1. Read Data Test PCA Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1, 2, 3	0180-0374	CAPACITOR, fxd, Ta, 10 μF, 20V	56289	150D106X9020B2-DYS
C4	0180-0100	CAPACITOR, fxd, elect, 4.7 μF, 35V	56289	150D475X9035B2-DYS
C5, 6	0160-2055	CAPACITOR, fxd, cer, 0.01 μF	56289	C023F101F103ZS22-CDH
CR1 thru CR6	1901-0040	DIODE, Si, 30V, 30 mA	07263	FDG1088
CR7 thru CR23	1990-0326	DIODE, visible light emitting	28480	1990-0326
R1, 15, 22, 23, 29, 30, 31, 37	0683-1025	RESISTOR, fxd, 1k, 1/4W	01121	CB-1025
R2, 16, 18	0683-4735	RESISTOR, fxd, 47k, 1/4W	01121	CB-4735
R3 thru R12, 17, 21, 24 thru R28	0683-1515	RESISTOR, fxd, 150 ohms, 1/4W	01121	CB-1515
R13, 19	0757-0418	RESISTOR, fxd, 619 ohms, 1/8W	19701	MF4CT-0
R14, 20, 32, 36	0757-0428	RESISTOR, fxd, 1.62k, 1%, 1/8W	19701	MF4CT-0
S1, 2	3101-1213	SWITCH, toggle	81640	T8201
U1	1820-1002	INTEGRATED CIRCUIT	01295	SN74104N
U2	1820-0281	INTEGRATED CIRCUIT	01295	SN74107N
U3	1820-0621	INTEGRATED CIRCUIT	01295	SN7438N
U4, 6, 8	1820-0577	INTEGRATED CIRCUIT	01295	SN7416N
U5	1820-0435	INTEGRATED CIRCUIT	04295	SN74180N
U7	1820-0515	INTEGRATED CIRCUIT	07263	U6B960259X
U9	1820-0207	INTEGRATED CIRCUIT	07263	U1A960159X



SIGNAL SUMMARY

MNEMONIC	SIGNAL NAME	MNEMONIC	SIGNAL NAME
$\overline{RDP}$	"Not" Read Data Parity Bit	$\overline{RC}$	"Not" Read Clock
$\overline{RD0}$	"Not" Read Data Bit 0	$\overline{EOB}$	"Not" End-of-Block
$\overline{RD1}$	"Not" Read Data Bit 1	$\overline{IDB}$	"Not" Identification Burst
$\overline{RD2}$	"Not" Read Data Bit 2	$\overline{TM}$	"Not" Tape Mark
$\overline{RD3}$	"Not" Read Data Bit 3	$\overline{MTE}$	"Not" Multiple Track Error
$\overline{RD4}$	"Not" Read Data Bit 4	$\overline{STE}$	"Not" Single Track Error
$\overline{RD5}$	"Not" Read Data Bit 5	$\overline{EOB(E)}$	"Not" End-of-Block (Extended)
$\overline{RD6}$	"Not" Read Data Bit 6	$\overline{CF}$	"Not" Command Forward
$\overline{RD7}$	"Not" Read Data Bit 7	$\overline{CR}$	"Not" Command Reverse
$\overline{SD16}$	"Not" PE Status		



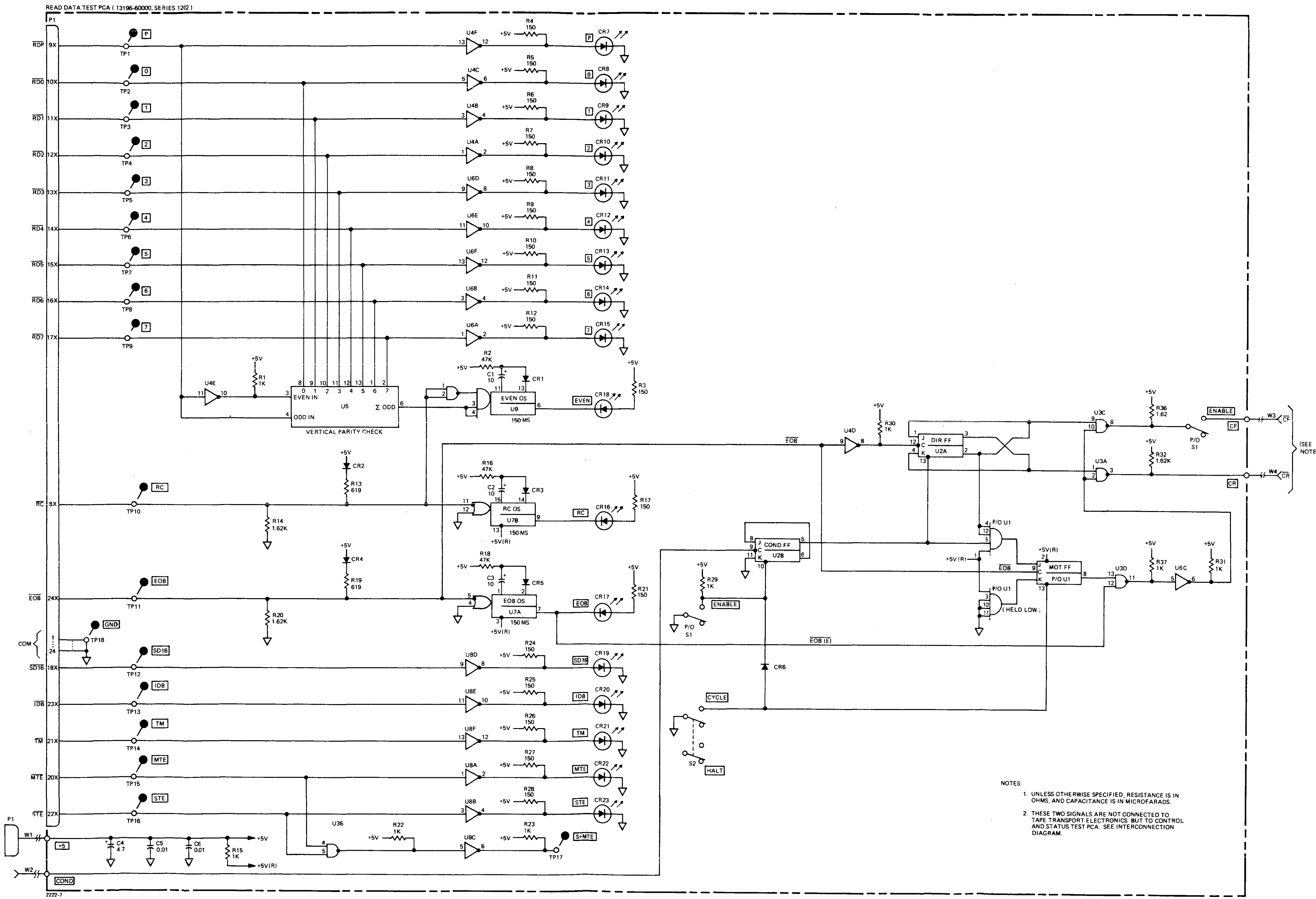
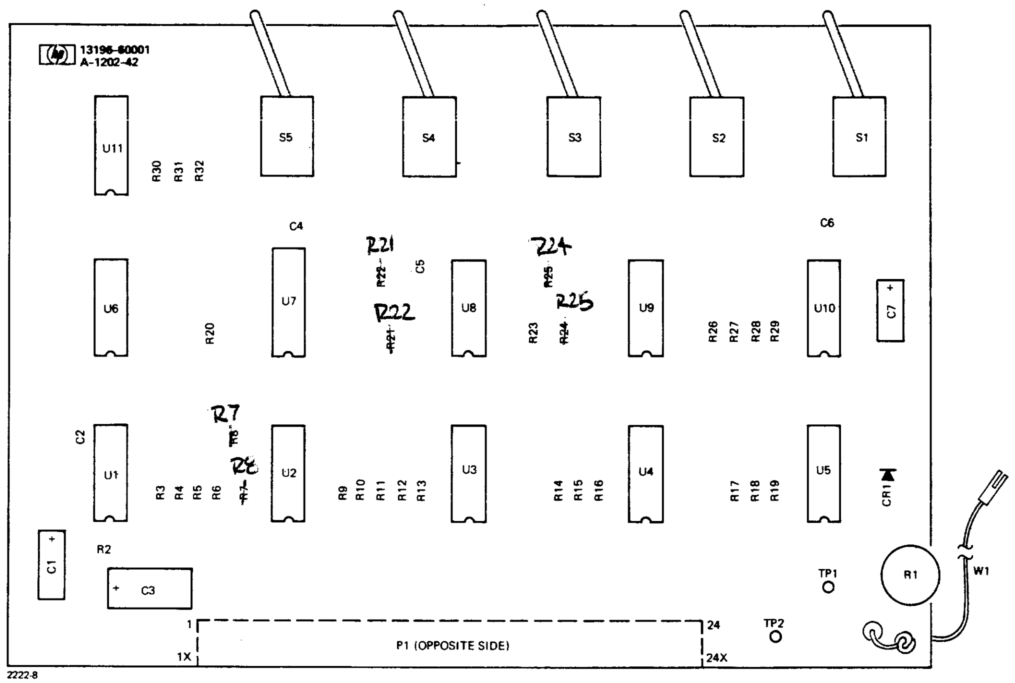


Figure 5-1. Read Data Test PCA Schematic and Parts Location Diagram

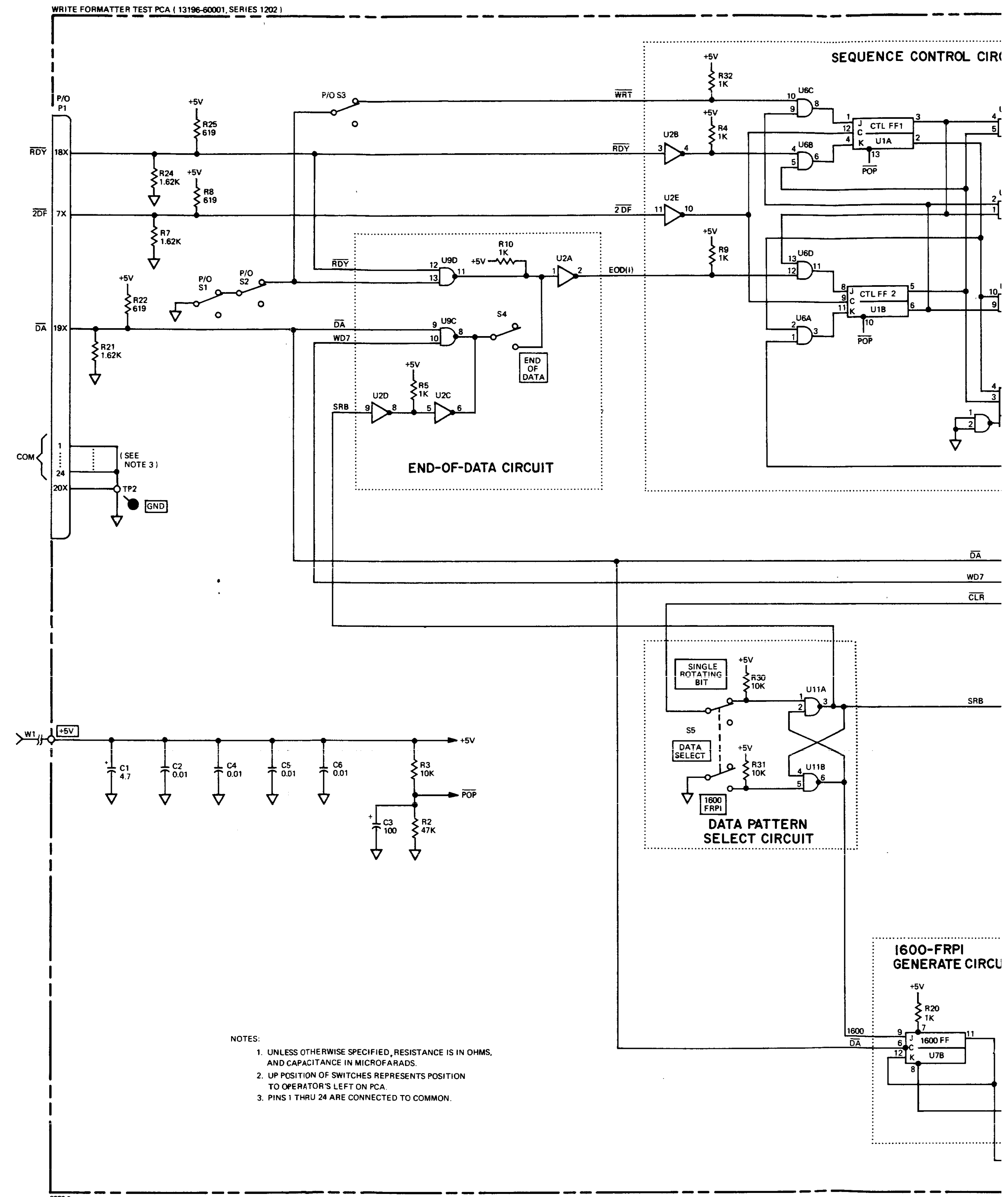
Table 5-2. Write Formatter Test PCA Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1	0180-0100	CAPACITOR, fxd, elect, 4.7 μF, 35V	56289	150D475X9035B2-DYS
C2, 4, 5, 6	0160-2055	CAPACITOR, fxd, cer, 0.01 μF	56289	C023F101F103ZS22-CDH
C3	0180-0061	CAPACITOR, fxd, 100 μF, 16V	56289	30D107G016DC2-DSM
C7	0180-0374	CAPACITOR, fxd, Ta, 10 μF, 20V	56289	150D106X9020B2-DYS
CR1	1901-0040	DIODE, Si, 30V, 30 mA	07263	FDG1088
R1 2100-1948	~~2100-3029~~	RESISTOR, var, 50k, 5% 28480	~~32997~~	~~M3365P-1-503~~ 2100-1
R2	0683-4735	RESISTOR, fxd, 47k, 1/4W	01121	CB-4735
R3, 30, 31	0683-1035	RESISTOR, fxd, 10k, 1/4W	01121	CB-1035
R4, 5, 6, 9, 10, 20, 27, 32, 33	0683-1025	RESISTOR, fxd, 1k, 1/4W	01121	CB-1025
R7, R11 thru R19, 21, 23, 24, 26, 28, 29	0757-0428	RESISTOR, fxd, 1.62k, 1%, 1/8W	19701	MF4CT-0
R8, 22, 25	0757-0418	RESISTOR, fxd, 619 ohms, 1/8W	19701	MF4CT-0
S1 thru S5	3101-1213	SWITCH, toggle	81640	T8201
U1	1820-0281	INTEGRATED CIRCUIT	01295	SN74107N
U2, 3, 4, 5	1820-0175	INTEGRATED CIRCUIT	01295	SN7405N
U6	1820-0141	INTEGRATED CIRCUIT	04713	SC7514PK
U7	1820-0076	INTEGRATED CIRCUIT	01295	SN4355
U8	1820-0294	INTEGRATED CIRCUIT	12040	SD9935
U9	1820-0621	INTEGRATED CIRCUIT	01295	SN7436N
U10	1820-0207	INTEGRATED CIRCUIT	07263	U1A960159X
U11	1820-0054	INTEGRATED CIRCUIT	01295	SN4342



SIGNAL SUMMARY

MNEMONIC	SIGNAL NAME	MNEMONIC	SIGNAL NAME
$\overline{RDY}$	"Not" Ready	$\overline{WPA}$	"Not" Write Preamble Command
$\overline{2DF}$	"Not" Twice Data Frequency	$\overline{WID}$	"Not" Write Identification Burst Command
$\overline{DA}$	"Not" Data Accepted	$\overline{WTM}$	"Not" Write Tape Mark Command
$\overline{WRT}$	"Not" Write	$\overline{WDP}$	"Not" Write Data Parity Bit
EOD(I)	End-of-Data (Internal)	$\overline{WD0}$	"Not" Write Data Bit 0
$\overline{POP}$	"Not" Power-On Preset	$\overline{WD1}$	"Not" Write Data Bit 1
$\overline{CEN}$	"Not" Command Enable	$\overline{WD2}$	"Not" Write Data Bit 2
$\overline{CLR}$	"Not" Clear	$\overline{WD3}$	"Not" Write Data Bit 3
SRB	Generate Single Rotating Bit Pattern	$\overline{WD4}$	"Not" Write Data Bit 4
1600	Generate 1600 FRPI Pattern	$\overline{WD5}$	"Not" Write Data Bit 5
$\overline{GAP}$	"Not" Insert Interrecord Gap	$\overline{WD6}$	"Not" Write Data Bit 6
$\overline{EOD}$	"Not" End-of-Data	$\overline{WD7}$	"Not" Write Data Bit 7



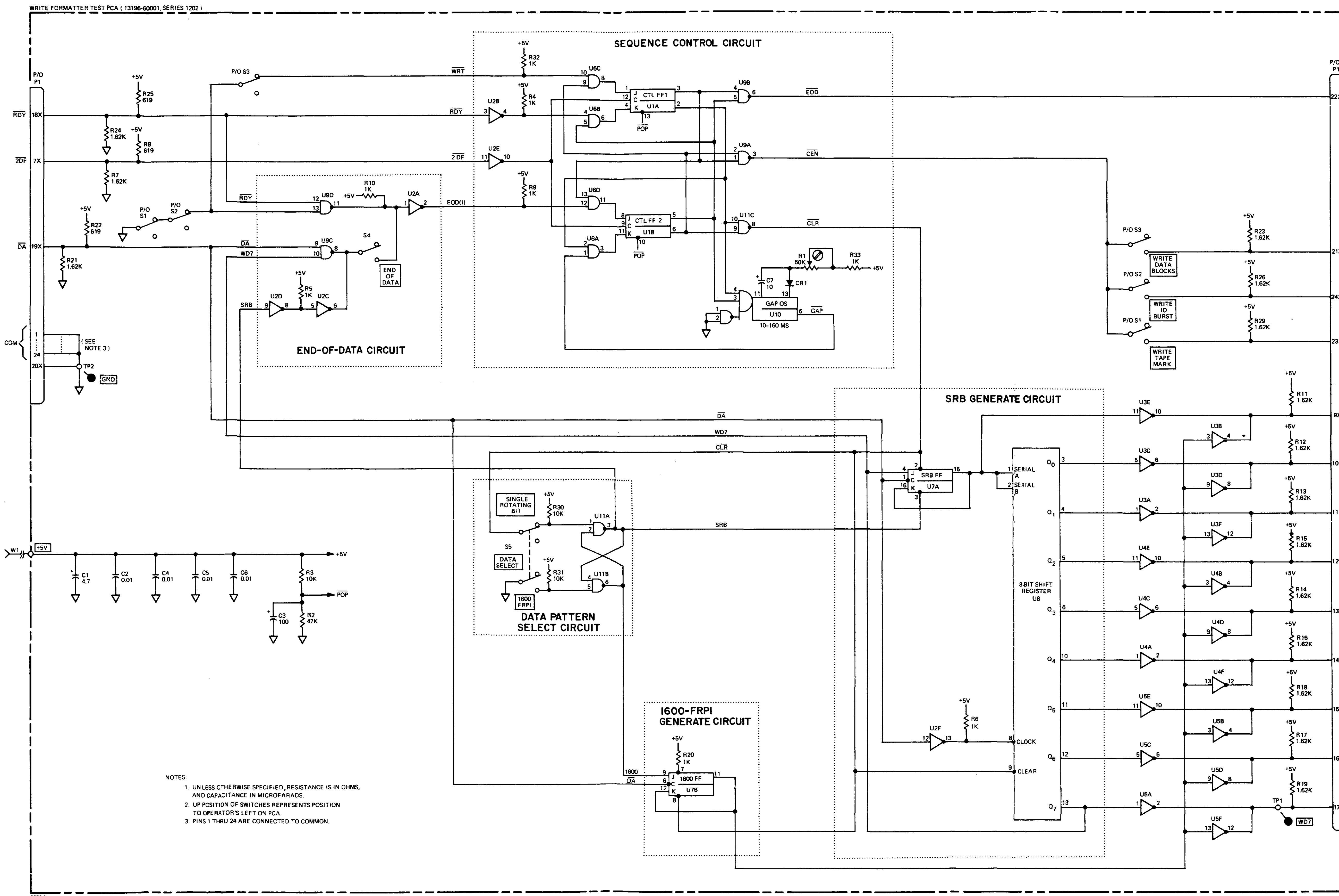


Figure 5-2. Write Formatter Test PCA Schematic and Parts Location Diagram

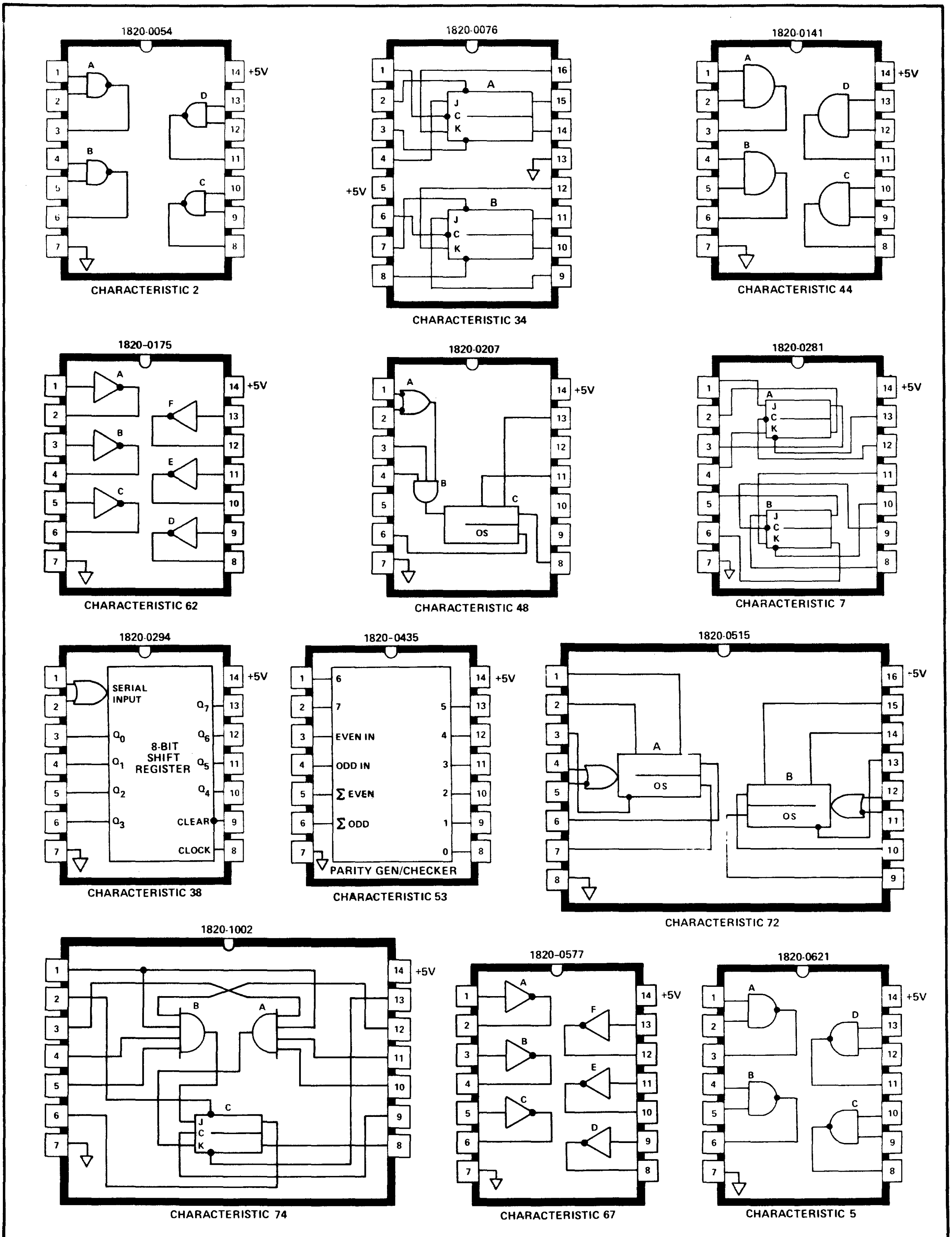


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Figure 5-3. Integrated Circuit Pack Diagrams

Table 5-3. Integrated Circuit Characteristics

CHARACTERISTIC NUMBER	INPUT VOLTAGE		OUTPUT VOLTAGE		OPEN INPUT ACTS AS	MAX. PROPAGATION DELAY	
	MINIMUM HIGH LEVEL	MAXIMUM LOW LEVEL	MINIMUM HIGH LEVEL	MAXIMUM LOW LEVEL		TO HIGH LEVEL (NS)	TO LOW LEVEL (NS)
2	2.0	0.8	2.4	0.4	Logic 1	29	15
5	2.0	0.8	(5)	0.4	Logic 1	45	15
7	2.0	0.8	2.4	0.4	Logic 1	50(2)	50
34	2.0(1)	0.8	2.4	0.4	Logic 1	30	45
38	2.0(3)	0.8	2.4	0.4	Logic 1	40	(4)
44	1.8	1.1	2.5	0.4	Logic 1	15	15
48	1.9	0.85	2.4	0.45	Logic 1	40	---
53	2.0	0.8	2.5	0.4	Logic 1	60	68
62	2.0	0.9	2.5	0.4	---	12	15
67	2.0	0.8	---	0.4	Logic 1	15	23
72	1.9	1.1	2.6	0.45	Logic 1	60	35
74	1.4	0.9	2.4	0.4	Logic 1	15	25

NOTES:

(1) Required pulse widths 16 ns min.

(2) Required clock pulse width 20 ns min; set-clear 25 ns min.

(3) Required clock and clear pulse width is typically 25 ns and 30 ns, respectively (45 ns max). Time serial A and B data must be set up prior to clock pulse, typically 15 ns (30 ns max).

(4) Delay is 40 ns clock to output and 50 ns clear to output.

(5) Level depends on load.

REPLACEABLE PARTS SECTION VI

6-1. INTRODUCTION.

6-2. This section contains information pertaining to replaceable parts for the HP 13196A and 13196A Option 001 Phase-Encoded Test Accessories. Included are replaceable parts lists and ordering information.

6-3. REPLACEABLE PARTS LISTS.

6-4. Table 6-1 lists the major replaceable parts for the test accessory. Table 6-2 is a further breakdown of replaceable parts for the test accessory. It lists the replaceable parts located on the test PCA's. The parts are in numerical order by part number. The total quantity of each part is specified for both the standard and the option 001 test accessories. Table 6-2 gives the following information for each part.

a. Hewlett-Packard part number.

b. Description of the part. (Refer to table 6-3 for an explanation of abbreviations used in the DESCRIPTION column.)

c. Manufacturer of the part, as a five-digit code. (Refer to table 6-4 for a listing of the manufacturers that correspond to the codes.)

d. Manufacturer's part number.

e. Total quantity of parts.

6-5. ORDERING INFORMATION.

6-6. To order replacement parts, address the order or inquiry to the local HP Sales and Service Office. (Refer to the list at the back of this manual.) Specify the following information for each part ordered.

a. Model number of accessory.

b. HP part number for each part.

c. Description of each part.

d. Circuit reference designation, if applicable. (Refer to tables 5-1 and 5-2 for reference designations.)

Table 6-1. Phase-Encoded Test Accessory Major Replaceable Parts

HP PART NO.	DESCRIPTION
13196-60000	READ DATA TEST PCA
13196-60001	WRITE FORMATTER TEST PCA (Part of option 001 only.)
13196-90000	OPERATING AND SERVICE MANUAL

Table 6-2. Phase-Encoded Test Accessory Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ	
				STD	OPT 001
0160-2055	CAPACITOR, fxd, cer, 0.01 μF	56289	C023F101F103ZS22-CDH	2	6
0180-0061	CAPACITOR, fxd, 100 μF, 16V	56289	30D107G016DC2-DSM	—	1
0180-0100	CAPACITOR, fxd, elect, 4.7 μF, 35V	56289	150D475X9035B2-DYS	1	2
0180-0374	CAPACITOR, fxd, Ta, 10 μF, 20V	56289	150D106X9020B2-DYS	3	4
0683-1025	RESISTOR, fxd, 1k, 1/4W	01121	CB-1025	8	17
0683-1035	RESISTOR, fxd, 10k, 1/4W	01121	CB-1035	—	3
0683-1515	RESISTOR, fxd, 150 ohms, 1/4W	01121	CB-1515	17	17
0683-4735	RESISTOR, fxd, 47k, 1/4W	01121	CB-4735	3	4
0757-0418	RESISTOR, fxd, 619 ohms, 1/8W	19701	MF4CT-0	2	5
0757-0428	RESISTOR, fxd, 1.62k, 1%, 1/8W	19701	MF4CT-0	4	20
1820-0054	INTEGRATED CIRCUIT	01295	SN4342	—	1
1820-0076	INTEGRATED CIRCUIT	01295	SN4355	—	1
1820-0141	INTEGRATED CIRCUIT	04713	SC7514PK	—	1
1820-0175	INTEGRATED CIRCUIT	01295	SN7405N	—	4
1820-0207	INTEGRATED CIRCUIT	07263	U1A960159X	1	2
1820-0281	INTEGRATED CIRCUIT	01295	SN74107N	1	2
1820-0294	INTEGRATED CIRCUIT	12040	SD9935	—	1
1820-0435	INTEGRATED CIRCUIT	01295	SN74180N	1	1
1820-0515	INTEGRATED CIRCUIT	07263	U6B960259X	1	1
1820-0577	INTEGRATED CIRCUIT	01295	SN7416N	3	3
1820-0621	INTEGRATED CIRCUIT	01295	SN7438N	1	2
1820-1002	INTEGRATED CIRCUIT	01295	SN74104N	1	1
1901-0040	DIODE, Si, 30V, 30 mA	07263	FDG1088	6	7
1990-0326	DIODE, visible light emitting	28480	1990-0326	17	17
2100-3029	RESISTOR, var, 50k, 5%	32997	M3365P-1-503	—	1
3101-1213	SWITCH, toggle	81640	T8201	2	7

Table 6-3. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly
B	= motor, synchro
BT	= battery
C	= capacitor
CB	= circuit breaker
CR	= diode
DL	= delay line
DS	= indicator
E	= Misc electrical parts
F	= fuse
FL	= filter
J	= receptacle connector
K	= relay
L	= inductor
M	= meter
P	= plug connector
Q	= semiconductor device other than diode or integrated circuit
R	= resistor
RT	= thermistor
S	= switch
T	= transformer
TB	= terminal board
TP	= test point
U	= integrated circuit, non-repairable assembly
V	= vacuum tube, photocell, etc.
VR	= voltage regulator
W	= jumper wire
X	= socket
Y	= crystal
Z	= tuned cavity, network

ABBREVIATIONS

A	= amperes
ac	= alternating current
Ag	= silver
Al	= aluminum
ar	= as required
adj	= adjust
assy	= assembly
b	= base
bp	= bandpass
bpi	= bits per inch
blk	= black
blu	= blue
brn	= brown
brs	= brass
Btu	= British thermal unit
Be Cu	= beryllium copper
cpi	= characters per inch
coll	= collector
cw	= clockwise
ccw	= counterclockwise
cer	= ceramic
com	= common
crt	= cathode-ray tube
CTL	= complementary-transistor logic
cath	= cathode
Cd pl	= cadmium plate
comp	= composition
conn	= connector
compl	= complete
dc	= direct current
dr	= drive
DTL	= diode-transistor logic
depc	= deposited carbon
dpdt	= double-pole, double-throw
dpst	= double-pole, single-throw
em	= emitter
ECL	= emitter-coupled logic
ext	= external
encap	= encapsulated
elctlt	= electrolytic
F	= farads
FF	= flip-flop
flh	= flat head
flm	= film
fxd	= fixed
filh	= fillister head
G	= giga (10^9)
Ge	= germanium
gl	= glass
gnd	= ground(ed)
gra	= gray
grn	= green
H	= henries
Hg	= mercury
hr	= hour(s)
Hz	= hertz
hdw	= hardware
hex	= hexagon, hexagonal
ID	= inside diameter
IF	= intermediate frequency
in.	= inch, inches
I/O	= input/output
int	= internal
incl	= include(s)
insul	= insulation, insulated
impgrg	= impregnated
incand	= incandescent
ips	= inches per second
k	= kilo (10^3), kilohm
lp	= low pass
m	= milli (10^{-3})
M	= mega (10^6), megohm
My	= Mylar
mfr	= manufacturer
mom	= momentary
mtg	= mounting
misc	= miscellaneous
met. ox.	= metal oxide
mintr	= miniature
n	= nano (10^{-9})
nc	= normally closed or no connection
Ne	= neon
no.	= number
n.o.	= normally open
np	= nickel plated
NPN	= negative-positive-negative
NPO	= negative-positive zero (zero temperature coefficient)
NSR	= not separately replaceable
NRFR	= not recommended for field replacement
OD	= outside diameter
OBD	= order by description
orn	= orange
ovh	= oval head
oxd	= oxide
p	= pico (10^{-12})
PC	= printed circuit
PCA	= printed-circuit assembly
PWB	= printed-wiring board
phh	= phillips head
pk	= peak
p-p	= peak-to-peak
pt	= point
prv	= peak inverse voltage
PNP	= positive-negative-positive
pwv	= peak working voltage
porc	= porcelain
posn	= position(s)
pozi	= pozidrive
rf	= radio frequency
rdh	= round head
rms	= root-mean-square
rwv	= reverse working voltage
rect	= rectifier
r/min	= revolutions per minute
RTL	= resistor-transistor logic
s	= second
SB, TT	= slow blow
Se	= selenium
Si	= silicon
scr	= silicon controlled rectifier
sst	= stainless steel
stl	= steel
spcl	= special
spdt	= single-pole, double-throw
spst	= single-pole, single-throw
Ta	= tantalum
td	= time delay
Ti	= titanium
tgl	= toggle
thd	= thread
tol	= tolerance
TTL	= transistor transistor logic
U(μ)	= micro (10^{-6})
V	= volt(s)
var	= variable
vio	= violet
Vdcw	= direct current working volts
W	= watts
ww	= wirewound
wht	= white
WIV	= working inverse voltage
yel	= yellow

Table 6-4. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and the latest supplements.

Code No.	Manufacturer	Address	Code No.	Manufacturer	Address
01121	Allen-Bradley Co.	Milwaukee, Wis.	12040	National Semiconductor Corp.	Danbury, Conn.
01295	Texas Instruments Inc., Semiconductor Components Division	Dallas, Texas	19701	Electra Mfg. Co.	Independance, Kansas
04713	Motorola Semiconductor Products Inc.	Phoenix, Arizona	28480	Hewlett-Packard Co.	Palo Alto, Calif.
07263	Fairchild Camera Inst. Corp., Semiconductor Div.	Mountain View, Calif.	32997	Bourns Inc., Trimpot Prod. Div.	Riverside, Calif.
			56289	Sprague Electric Company	N. Adams, Mass.
			81640	Controls Company of America, Control Switch Div.	Folcroft, Pa.

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